UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,534	11/07/2005	Franz Hoffman	1432.120101/P30123	4775

25281 7590 10/10/2008

DICKE, BILLIG & CZAJA
FIFTH STREET TOWERS
100 SOUTH FIFTH STREET, SUITE 2250
MINNEAPOLIS, MN 55402

EXAMINER	
PARENDO, KEVIN A	
ART UNIT	**PAPER NUMBER**
2823	

MAIL DATE	DELIVERY MODE
10/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,534	HOFFMAN ET AL.	
	Examiner	Art Unit	
	Kevin A. Parendo	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/3/05 and 8/23/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action for application number 10/537534 is in response to an application filed on 11/7/05.

Drawings

2. The drawings are objected to because it appears that 312 in Fig. 3B should point instead to the region attached to the top of 311; the thin region that 312 points to appears to be incorrectly included in both Fig. 3B and Fig. 3D and should be removed. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Memory cell having voltage-controlled bridging structure.

Claim Objections

4. Claims 20, 33, 36, and 41 are objected to because they contain the limitation “the distance" on lines 8, 9, 11, and 9, respectively. This limitation has not been claimed previously to this instance and thus lacks proper antecedent basis. To avoid any ambiguity, the word "the" in this limitation should be change to "a".

5. Claims 20, 21, 33, and 36 are objected to because they contain the limitation “the electrically conductive regions " on lines 13-14 of claim 20, on line 3 of claim 21, on lines 8, 9, 10, 11, and 12 of claim 33, and 10, 11, 12, 13, and 14 of claim 36. This limitation has not been claimed previously to this instance and thus lacks proper antecedent basis. To avoid any ambiguity, the limitation should be amended to “the first and second electrically conductive regions.”

6. Claim 25 is objected to because it contains the typographical error “to be 0.5 nm and 5 nm” on line 3. This is a range and thus the limitation should be amended to "to be between 0.5 nm and 5 nm.”

7. Claim 27 is objected to because it contains the typographical error “interconnect, which interconnects” on line 2. The limitation should be amended to “interconnect, in which the first and second interconnects" both for grammatical correctness, and the first and second should be included to match the language of lines 1-2 of claim 27.

8. Claim 27 is objected to because the term "substantially" is a relative term (one definition of "substantial" is “being largely but not wholly that which is specified”) that renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Appropriate correction is required.

9. Claims 32 and 35 are objected to because they contain the limitation and/or in the group, which is confusing and ambiguous as to whether the group can be silver, copper, aluminum or gold, or if it can be platinum. The "and/or" should be amended to "and" to include all elements in the group.

10. Claims 33, 36, and 41 are objected to because the limitation “prescribable distance” is confusing and ambiguous, as it is unclear as what “prescribable” refers to. A quick search of Webster’s Dictionary (m-w.com) gives the definition of prescribe as “to lay down a rule” or alternatively as “to write prescription.” It is unclear as to what rule is meant. Appropriate correction is required.

11. Claims 33, 36, and 41 are objected to because the limitation “freely growing fashion” is confusing and ambiguous, as it is unclear as what “freely” refers to. Appropriate correction is required.

12. Claims 33, 36, and 41 are objected to because the limitation “freely growing fashion” is confusing and ambiguous, as it is unclear as what “freely” refers to. Appropriate correction is required.

13. Claim 25 is objected to because it contains the typographical error “comprising wherein” that should be amended to “wherein.”

14. Claim 41 is objected to because it contains the limitation “the electrically conductive means" on lines 8, 9, 10, 11, and 12. This limitation has not been claimed previously to this instance and thus lacks proper antecedent basis. Since means can be singular or plural, this creates ambiguity as to whether the first electrically conductive means, the second electrically conductive means, or both, is intended. To avoid any

ambiguity, the limitation should be amended to "the first and second electrically conductive means."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 33-39 and 41 are rejected under 35 U.S.C. 102(b) as being anticipated by Kozicki et al. (US 6,084,796, hereinafter "Kozicki").

Re claim 33, Kozicki discloses a binary information memory cell comprising:

- a substrate **61** (column 10, line 57 and Fig. 6B);
- a first electrically conductive region **63** (column 10, lines 61-62 and Fig. 6B) associated with the substrate;
- a second electrically conductive region **64** (column 11, lines 7-8 and Fig. 6B) arranged at a prescribable distance from the first electrically conductive region such that a cavity (via hole, that is filled with fast ion conductor **62**, column 10, lines 62-67 and Fig. 6B) is formed between the first and second electrically conductive regions; and
- wherein the first and second electrically conductive regions are set up such that upon application of a first voltage to the electrically conductive

regions a structure **65** (dendrite, column 11, lines 14-17 and Fig. 6B) which at least partially bridges the distance between the electrically conductive regions is formed in freely growing fashion from material from at least one of the electrically conductive regions (column 3, lines 25-55).; and upon application of a second voltage to the electrically conductive regions material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back (column 3, lines 25-55).

Re claim 34, Kozicki discloses that the first or the second electrically conductive region is made of metallic material (anode is silver, cathode is aluminum, see column 3, lines 36-38).

Re claim 35, Kozicki further discloses that the first or the second electrically conductive region is made of at least one material from a group consisting of silver, copper, aluminum, gold and/or platinum (anode is silver, cathode is aluminum, see column 3, lines 36-38).

Re claim 36, Kozicki discloses a binary information memory cell arrangement comprising:

- a plurality of binary information memory cells (MDM's in an array, see column 11, lines 62-63) having one or more memory cells comprising:
- a substrate **61** (column 10, line 57 and Fig. 6B);
- a first electrically conductive region **63** (column 10, lines 61-62 and Fig. 6B) associated with the substrate;

- a second electrically conductive region **64** (column 11, lines 7-8 and Fig. 6B) arranged at a prescribable distance from the first electrically conductive region such that a cavity (via hole, that is filled with fast ion conductor **62**, column 10, lines 62-67 and Fig. 6B) is formed between the first and second electrically conductive regions; and
- wherein the first and second electrically conductive regions are set up such that upon application of a first voltage to the electrically conductive regions a structure **65** (dendrite, column 11, lines 14-17 and Fig. 6B) which at least partially bridges the distance between the electrically conductive regions is formed in freely growing fashion from material from at least one of the electrically conductive regions (column 3, lines 25-55).; and upon application of a second voltage to the electrically conductive regions material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back (column 3, lines 25-55).

Re claim 37, Kozicki further discloses that the binary information memory cells are arranged in matrix form (the MDMs are formed in an array, see column 11, lines 62-63).

Re claim 38, Kozicki further discloses that selection elements for selecting a binary information memory cell are produced in and/or on the substrate for at least some of the binary information memory cells (column 13, lines 7-13).

Re claim 39, Kozicki further discloses that the selection elements are field effect transistors (column 13, lines 7-13).

Re claim 41, Kozicki discloses a binary information memory cell comprising:

- a substrate **61** (column 10, line 57 and Fig. 6B);
- a first electrically conductive means **63** (column 10, lines 61-62 and Fig. 6B) associated with the substrate;
- a second electrically conductive means **64** (column 11, lines 7-8 and Fig. 6B) arranged at a prescribable distance from the first electrically conductive means such that a cavity (via hole, that is filled with fast ion conductor **62**, column 10, lines 62-67 and Fig. 6B) is formed between the first and second electrically conductive means; and
- wherein the first and second electrically conductive means are set up such that upon application of a first voltage to the electrically conductive means a structure **65** (dendrite, column 11, lines 14-17 and Fig. 6B) which at least partially bridges the distance between the electrically conductive means is formed in freely growing fashion from material from at least one of the electrically conductive means (column 3, lines 25-55); and upon application of a second voltage to the electrically conductive means material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back (column 3, lines 25-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 20-21 and 25-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki in view of Vogeli (US 2004/0087162 A1).

Re claim 20, Kozicki discloses a method for producing a binary information memory cell comprising:

- producing a first electrically conductive region **63** (column 10, lines 61-62 and Fig. 6B) associated with a substrate **61** (column 10, line 57 and Fig. 6B);
- producing an auxiliary structure (insulating layer **66** is deposited and etched to form a via hole **69**, and filled with fast ion conductor **62**, so this etched portion is auxiliary, column 10, lines 62-67 and Fig. 6B) of a prescribed thickness on the first electrically conductive region;
- producing a second electrically conductive region **64** (column 11, lines 7-8 and Fig. 6B) on the auxiliary structure;
- so that a cavity (via hole, that is filled with fast ion conductor **62**, column 10, lines 62-67 and Fig. 6B) is formed between the first electrically conductive region and the second electrically conductive region; and
- configuring the first and second electrically conductive regions such that upon applying a first voltage to the first and second electrically conductive

regions a structure **65** (dendrite, column 11, lines 14-17 and Fig. 6B) which at least partially bridges the distance between the first and second electrically conductive regions is formed from material from at least one of the electrically conductive regions.

Re claim 20, Kozicki fails to disclose removing the auxiliary structure after the second electrically conductive region has been produced, and that the distance between the first electrically conductive region and the second electrically conductive region corresponding to a tunnel spacing. Vogeli discloses removing an auxiliary structure **216** (paragraph 27 and Fig. 2A) after it has been covered (by **220**), to form a cavity **224** (paragraph 28). Vogeli also discloses that the distance is a tunnel spacing ("nanoscopic void", paragraph 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the covering of the auxiliary material as a method of forming a cavity, as well as the spacing of the cavity, of Vogeli, to the invention of Kozicki. The motivation to do so is that the combination produces the predictable results of forming a cavity with a nanoscopic dimension of between 1 nm and 1000 nm, Involving monolayer deposition (paragraph 12).

Re claim 21, Kozicki further discloses that applying a second voltage to the electrically conductive regions, material from the structure which at least partially bridges the distance between the electrically conductive regions is taken back (column 3, lines 25-55).

Re claims 25-26, Kozicki and Vogeli disclose the limitations of claim 20, as discussed above, but Kozicki fails to further disclose defining the distance between the

first conductive region and the second conductive region to be 0.5 nm and 5 nm (claim 25) or to be between 0.6 nm and 2 nm (claim 26). Vogeli discloses forming the distance to be between 1 nm and 1000 nm (paragraph 12). It would have been obvious to one of ordinary skill in the art at the time of invention to add the distance of Vogeli to the invention of Kozicki. The motivation to do so is that the combination produces the predictable results of forming a cavity with a nanoscopic dimension of between 1 nm and 1000 nm, Involving monolayer deposition (paragraph 12).

Re claim 27, Kozicki further discloses that the first electrically conductive region is a first interconnect and the second electrically conductive region is a second interconnect, which interconnects are produced so as to run toward one another at substantially right angles (column 11, lines 10-11).

Re claim 28, Kozicki further discloses defining the substrate to be a silicon substrate (column 49).

Re claim 29, Kozicki further discloses forming the first electrically conductive region or the second electrically conductive region from at least one material from a group consisting of a solid-state electrolyte, a glass comprising metal ions, a semiconductor comprising metal ions, or a chalcogenide (column 3, lines 25-28).

Re claim 30, Kozicki further discloses forming the first electrically conductive region or the second electrically conductive region from silver sulfide (column 3, lines 34-36; since no chemical formula is given, arsenic trisulphide-silver is considered a “silver sulfide.”).

In any case: the Applicant has not disclosed that the claimed material is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add the claimed material to the invention, since such a material would have been discovered during routine experimentation and optimization. See, for example, MPEP 2144.03, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizaka*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992). An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Re claim 31, Kozicki further discloses forming the first electrically conductive region or the second electrically conductive region from metal material (anode is silver, cathode is aluminum, see column 3, lines 36-38).

Re claim 32, Kozicki further discloses forming the first electrically conductive region or the second electrically conductive region from at least one material from a group consisting of silver, copper, aluminum, gold and/or platinum (anode is silver, cathode is aluminum, see column 3, lines 36-38).

17. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki and Vogeli as applied to claim 20 above, and further in view of Requicha et al. (US 6,508,979 B1, hereinafter Requicha).

Re claim 22, Kozicki and Vogeli disclose the limitations of claim 20 but fail to further disclose defining the auxiliary structure to be a self-assembled monolayer. Requicha disclose a self-assembled monolayer **210** that is used as a sacrificial "auxiliary structure" (column 3, lines 3-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the self-assembled monolayer of Requicha to the invention of Kozicki. The motivation to do so is that the combination produces the predictable results of forming a sacrificial layer in a well-ordered pattern (column 1, lines 43-45) of only about a monolayer thickness (column 3, line 1).

18. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki and Vogeli as applied to claim 20 above, and further in view of Jin et al. (US 2002/0175385 A1, hereinafter “Jin”).

Re claim 23, Kozicki and Vogeli disclose limitations of claim 20, as discussed above, but fail to further disclose producing the auxiliary structure using an atomic layer

deposition method. Jin discloses producing an auxiliary structure (sacrificial spacer, paragraph 18) using an atomic layer deposition method. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the atomic layer deposition of Jin to the invention of Kozicki. The motivation to do so is that the combination produces the predictable results of forming a sacrificial layer with a thickness on the order of 200-600 Angstroms (paragraph 18).

19. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki and Vogeli as applied to claim 20 above, and further in view of King et al. (US 2004/0222357 A1, hereinafter "King").

Re claim 24, Kozicki and Vogeli disclose the limitations of claim 20, as discussed above, but fail to further disclose producing the auxiliary structure using a molecular beam epitaxy method. King discloses producing an auxiliary structure (sacrificial layer 22, paragraph 14) by molecular beam epitaxy. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the atomic layer deposition of Jin to the invention of Kozicki. The motivation to do so is that the combination produces the predictable results of forming a sacrificial layer using a method that is well known to produce nanometer-scale thick films that are epitaxially ordered.

20. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki and Vogeli as applied to claim 39 above, and further in view of Bissey et al. (US 2004/0041188 A1, hereinafter "Bissey").

Re claim 40, Kozicki and Vogeli disclose the limitations of claim 39, as discussed above, but fail to further disclose that the selection elements are vertical field effect transistors. Bissey discloses controlling a memory cell 12 with a vertical FET (paragraph 23). . It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the vertical FET of Bissey to the invention of Kozicki. The motivation to do so is that the combination produces the predictable results creating a FET that takes up less space due to its vertical orientation (paragraph 23).

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Parendo, whose can be contacted by phone at (571) 270-5030 or directly by fax at (571) 270-6030. The examiner can normally be reached on Mon.-Thurs. 7:30 a.m. - 5:00 p.m. ET and on alternate Fridays 7:30 a.m. – 4:00 p.m. ET.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michelle Estrada/
Primary Examiner, Art Unit 2823

Kevin A. Parendo, Ph.D.
Examiner, Art Unit 2823

/Kevin A. Parendo/
10/10/2008